HTM0144A01

产品名称（**Product name**） ： 彩色 TFT LCD 模组

型　　号（**Model**） ： HTM0144A01

编　　号（**Part number**） ： 20160714001

日　　期（**Date**） ： 2016-07-14

深圳市鑫洪泰电子科技有限公司 Shenzhen Hot Display Technology Co.,Ltd		
编制 Prepared by	审核 Checked by	核准 Approved by

编码：QR-R-011　A/0　　序号：

Rev.	Descriptions	Date
01	Prelimiay Release	2016-07-15

1. Basic Specifications

1.1 Display Specifications

1>LCD Display Mode	128*RGB*128, 262K-Color TFT , Normal Black VA
2>Viewing Angle	Wide View
3>Driving Method	TFT Active Matrix
4>Interface	SPI-4 Interface
5>Backlight:	2Pcs White LED
6>Controller/Driver	**ST7735**

1.2 Mechanical Specifications

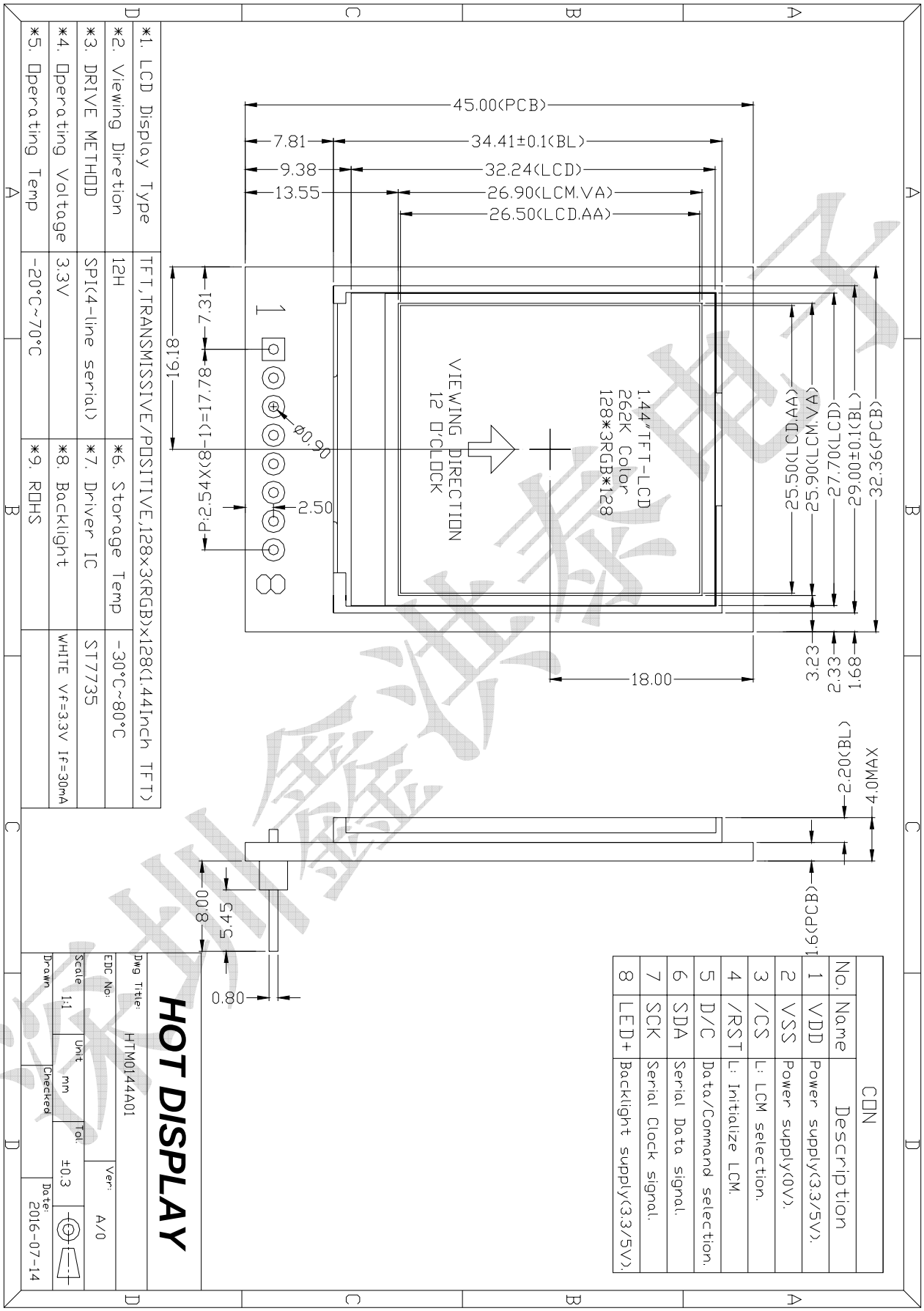
1>Outline Dimension	45.0(L)x32.36(W)x4(H)mm(Detailed Information refer to LCM Drawing)
2>Active Area	26.5(L)x25.5(W)
3>View Area	26.9(L)x25.9(W)

2. Terminal Function

CON:

Pin No.	Pin Name	Function
1	VDD	Power supply(3.3V/5V).
2	VSS	Power supply(0V).
3	/CS	L: LCM selection.
4	/RST	L:Initialize LCM.
5	D/C	Data/Command selection.
6	SDA	Serial Data signal.
7	SCK	Serial Clock signal.
8	LED+	Backlight supply(3.3V/5V).

3. Mechanical Specifications


45.00(PCB)
34.41±0.1(BL)
32.24(LCD)
26.90(LCM.VA)
26.50(LCD.AA)
7.81
9.38
13.55
81.91
17.78(1)=17.78
P:2.54X(8-1)=17.78
ø0.90
2.50
7.31
VIEWING DIRECTION
12 O'CLOCK
1.44"TFT-LCD
262K Color
128*3RGB*128
25.50(LCD.AA)
25.90(LCM.VA)
27.70(LCD)
29.00±0.1(BL)
32.36(PCB)
18.00
3.23
2.33
1.98
2.20(BL)
4.0MAX
1.6(PCB)
8.00
5.45
0.80
*1. LCD Display Type
TFT,TRANSMISSIVE/POSITIVE,128×3(RGB)×128(1.44Inch TFT)
*2. Viewing Direction
12H
*3. DRIVE METHOD
SPI(4-line serial)
*4. Operating Voltage
3.3V
*5. Operating Temp
-20°C~70°C
*6. Storage Temp
-30°C~80°C
*7. Driver IC
ST7735
*8. Backlight
WHITE Vf=3.3V If=30mA
*9. ROHS
CON
No.
Name
Description
1 VDD Power supply(3.3/5V).
2 VSS Power supply(0V).
3 /CS L: LCM selection.
4 /RST L: Initialize LCM.
5 D/C Data/Command selection.
6 SDA Serial Data signal.
7 SCK Serial Clock signal.
8 LED+ Backlight supply(3.3/5V).
HOT DISPLAY
Dwg Title: HTM0144A01
EDC No:
Scale 1:1
Unit mm
Tol. ±0.3
Ver: A/0
Drawn
Checked
Date: 2016-07-14

4. Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	-0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +1.95	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic input voltage range	VIN	0.3 ~ VDDI +0.3	V
Logic output voltage range	VO	0.3 ~ VDDI +0.3	V
Operating temperature range	TOPR	−20 ~ 70	℃
Storage temperature range	TSTG	-30 ~ 80	℃

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

5. Electrical Characteristics

5.1 DC Characteristics

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	Typ	Max		
Power & operation voltage							
System voltage	VDD	Operating voltage	2.6	2.75	3.3	V	
Interface operation voltage	VDDI	I/O supply voltage	1.65	1.9	3.3	V	
Gate driver high voltage	VGH		10		15	V	
Gate driver low voltage	VGL		-12.4		-7.5	V	
Gate driver supply voltage		| VGH-VGL |	17.5		27.5	V	
Input / Output							
Logic-high input voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-low input voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-high output voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-low output voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-high input current	IIH	VIN = VDDI			1	uA	Note 1

Logic-low input current	IIL	VIN = VSS	-1			uA	Note 1
Input leakage current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM voltage							
VCOM high voltage	VCOMH	Ccom=12nF	2.5		5.0	V	
VCOM low voltage	VCOML	Ccom=12nF	-2.4		0.0	V	
VCOM amplitude	VCOMAC	|VCOMH-VCOML|	4.0		6.0	V	
Source driver							
Source output range	Vsout		0.1		AVDD-0.1	V	
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	Tr	Below with 99% precision			20	us	Note 2
Output offset voltage	Voffset				35	mV	Note 3

Notes:

1. VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, TA= -20 to 70℃

2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.

3. The Max. value is between measured point of source output and gamma setting value.

5.2 Timing chart

5.2.1 4-line serial interface characteristics

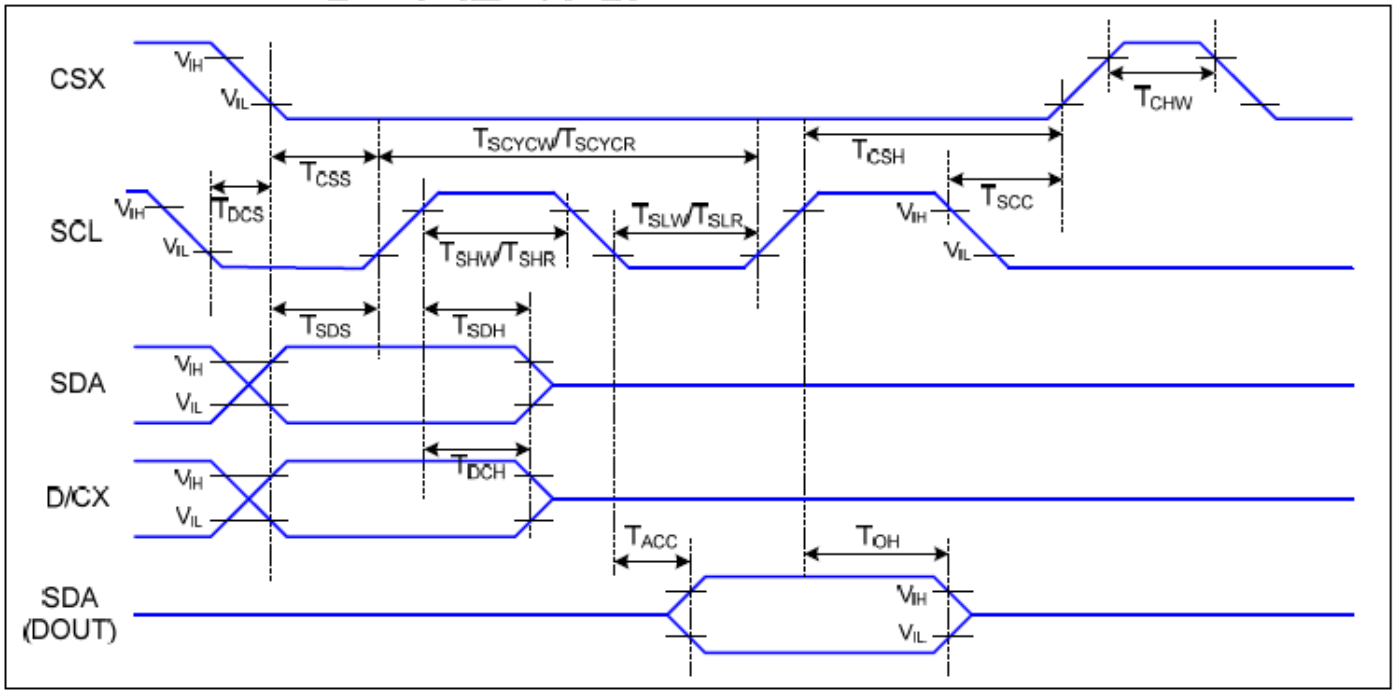


Fig.5.2.1 4-line serial interface timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time (write)	15		ns	
	TCSH	Chip select hold time (write)	15		ns	
	TCSS	Chip select setup time (read)	60		ns	
	TSCC	Chip select hold time (read)	65		ns	
	TCHW	Chip select "H" pulse width	40		ns	
SCL	TSCYCW	Serial clock cycle (Write)	66		ns	-write command & data ram
	TSHW	SCL "H" pulse width (Write)	30		ns	
	TSLW	SCL "L" pulse width (Write)	30		ns	
	TSCYCR	Serial clock cycle (Read)	150		ns	-read command & data ram
	TSHR	SCL "H" pulse width (Read)	60		ns	
	TSLR	SCL "L" pulse width (Read)	60		ns	
D/CX	TDCS	D/CX setup time		0	ns	
	TDCH	D/CX hold time	10		ns	
SDA (DIN) (DOUT)	TSDS	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	TSDH	Data hold time	10		ns	
	TACC	Access time	10	50	ns	
	TOH	Output disable time		50	ns	

Table 5.2.1 4-line Serial Interface Characteristics

Note 1: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 ℃

Note 2: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6. Function description

6.1 Write Functions

The write mode of the interface means the micro controller writes commands and data to the LCD driver. In 4-line serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

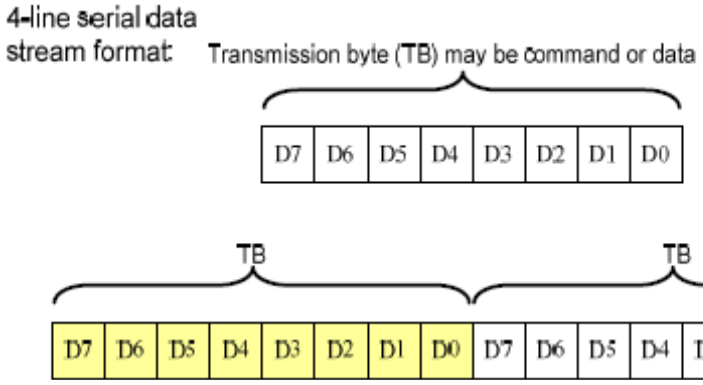


Fig. 6.1.1 Serial interface data stream format

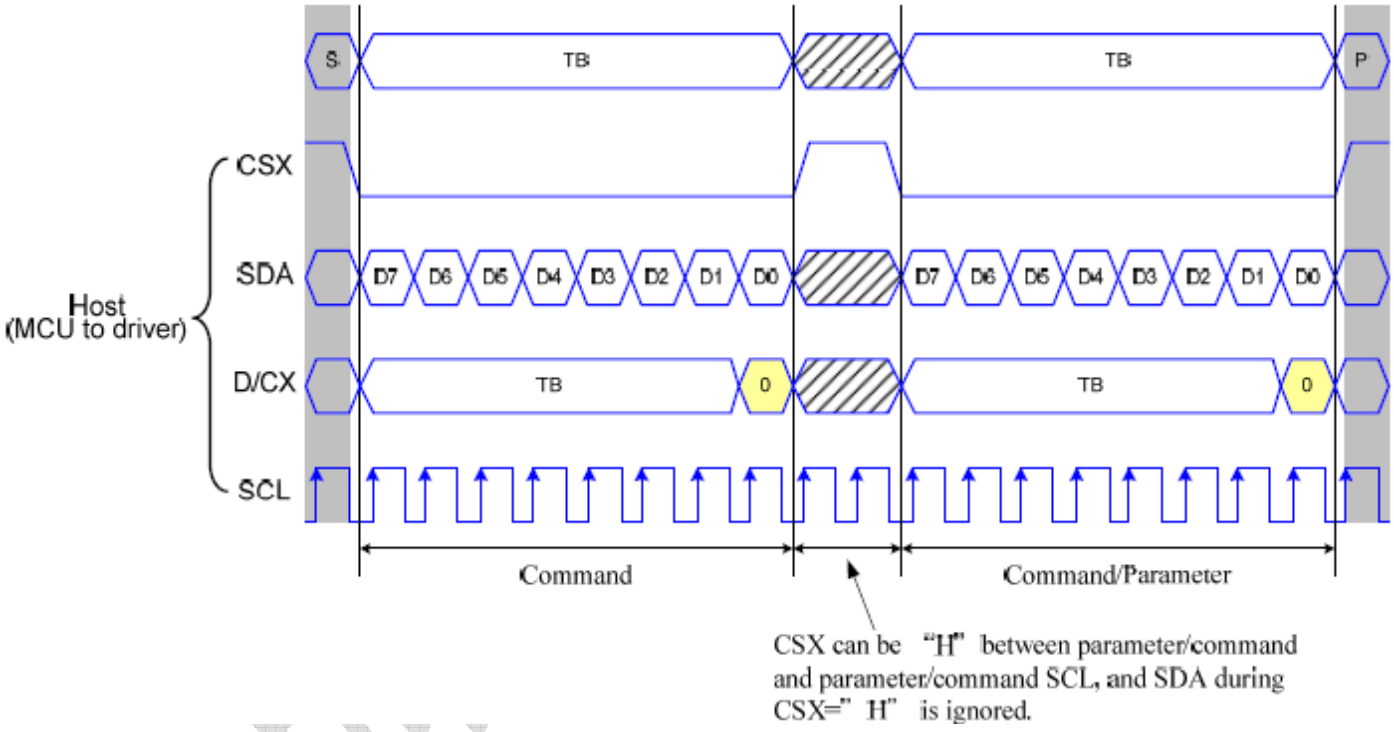


Fig. 6.1.2 4-line serial interface write protocol (write to register with control bit in transmission)

6.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL. After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

4-line serial protocol (for RDDID command: 24-bit read):

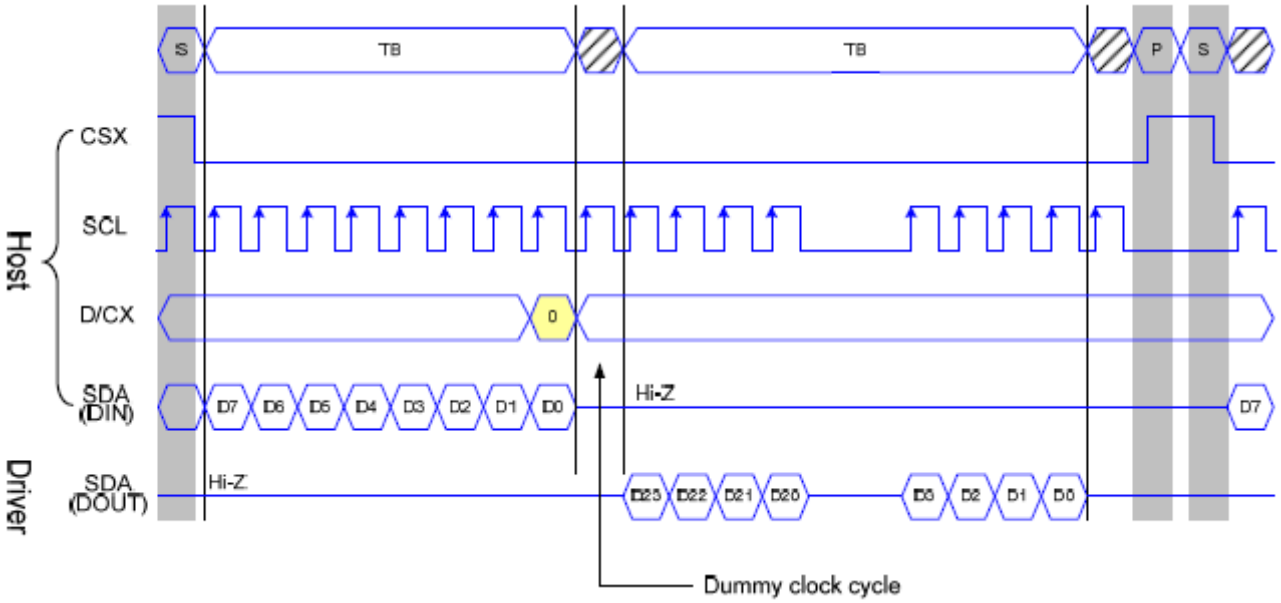


Fig. 6.2.1 4-line serial interface read protocol

6.3 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below. This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

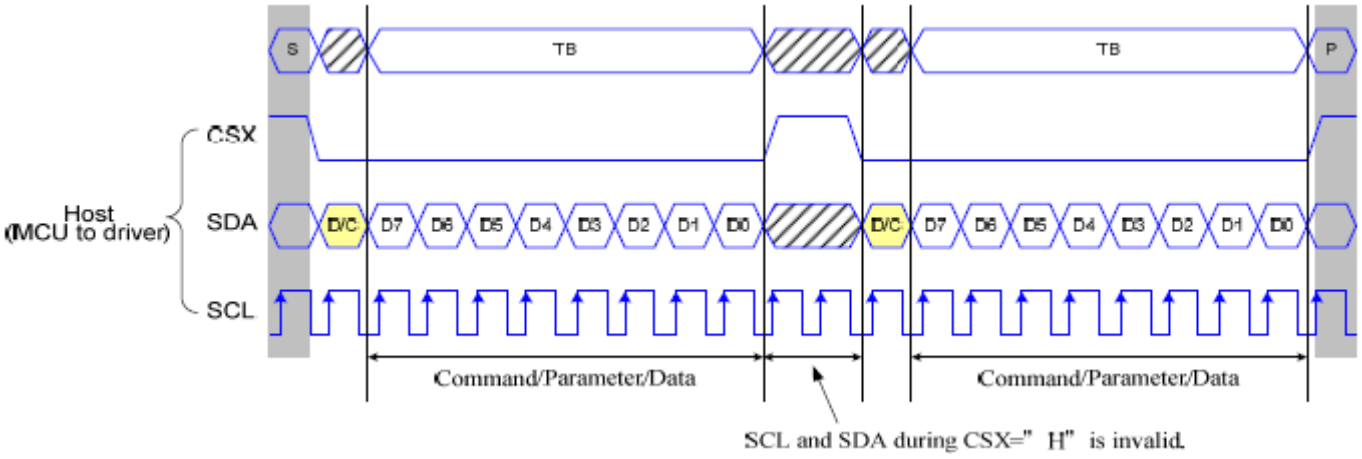


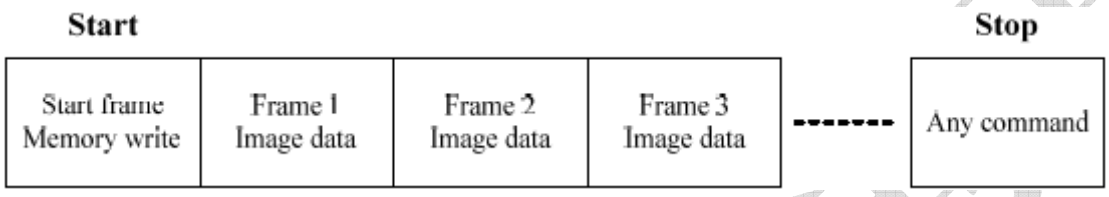
Fig. 6.3.1 Serial interface pause protocol (pause by CSX)

6.4 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

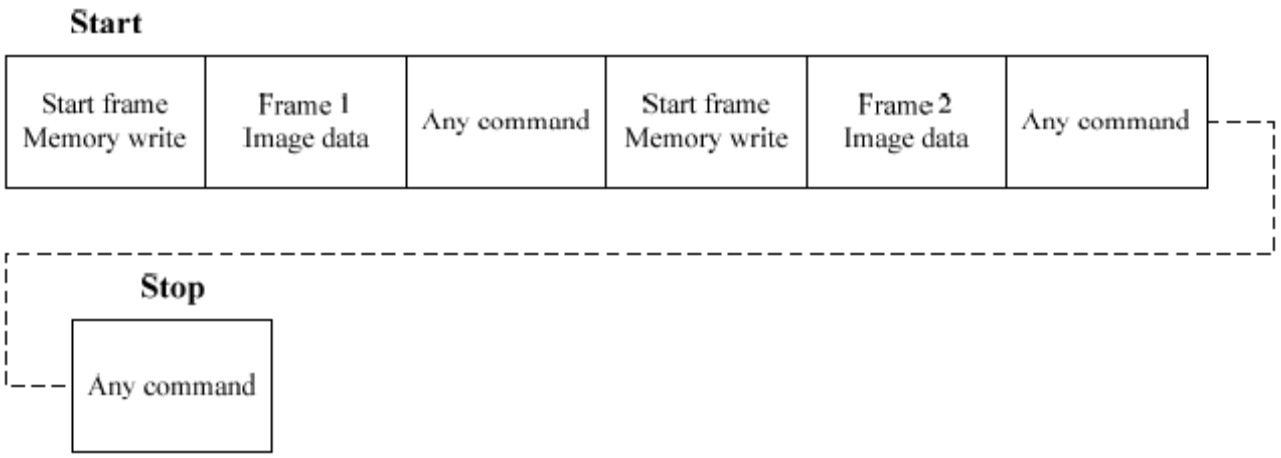
6.4.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



6.4.2 Method 2

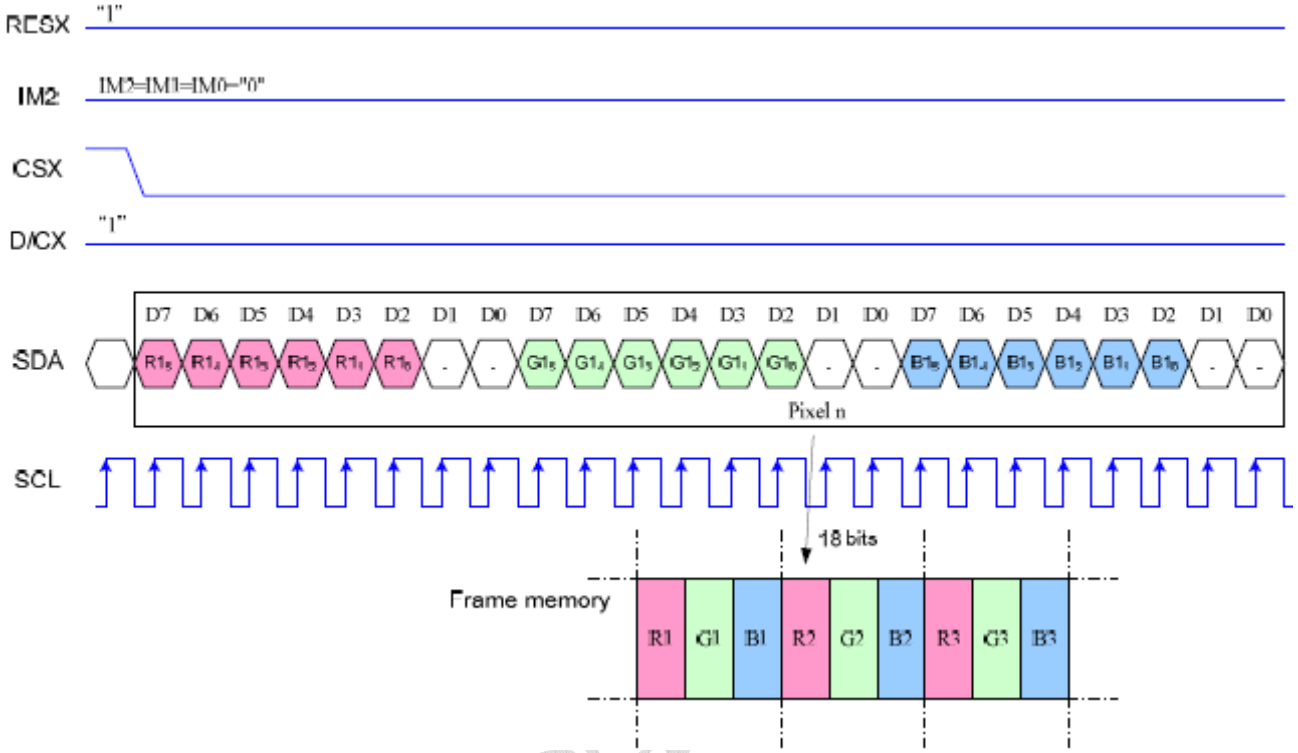
The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

6.5 Data Color Coding

Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1: Pixel data with the 18-bit color depth information
Note 2: The most significant bits are: Rx5, Gx5 and Bx5
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

6.6 Display Data RAM

6.6.1 Configuration (GM[2:0] = “000”)

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

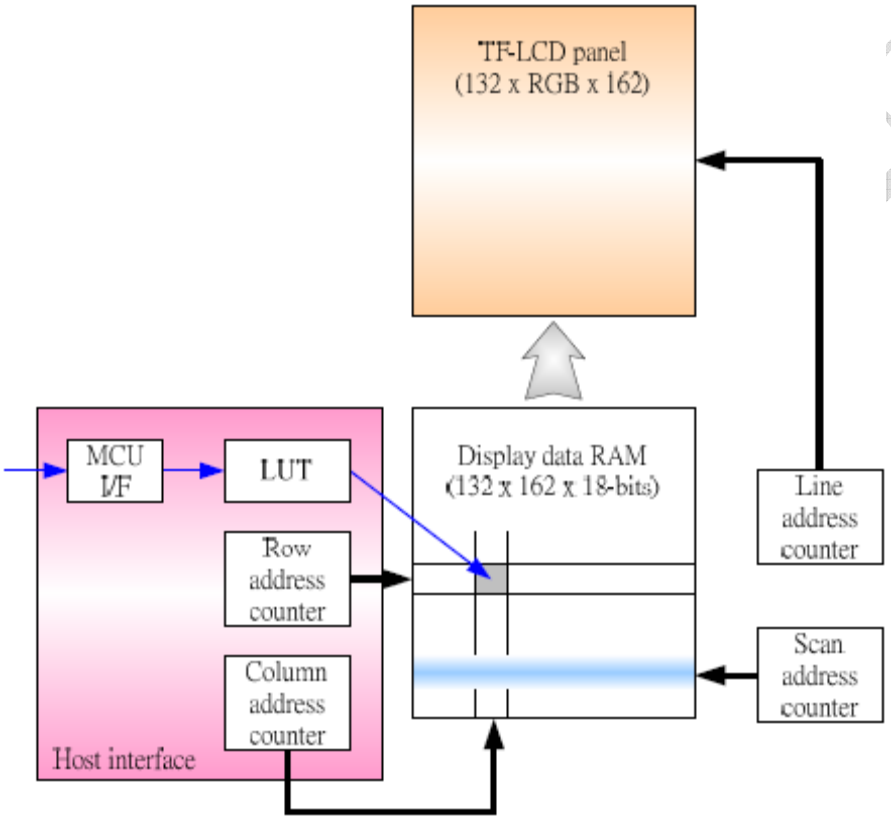


Fig. 6.6.1 Display data RAM organization

6.6.2 Memory to Display Address Mapping

6.6.2.1 When using 128RGB x 160 resolution (GM[2:0] = “011”, SMX=SMY=SRGB= ‘0’)

Gate Out	Source Out		S7	S8	S9	S10	S11	S12	-------	S385	S386	S387	S388	S389	S390		
	RA		RGB=0		RGB=1	RGB=0		RGB=1	RGB Order	RGB=0		RGB=1	RGB=0		RGB=1	SA	
	MY=' 0 '	MY=' 1 '														ML=' 0 '	ML=' 1 '
2	0	159	R0	G0	B0	R1	G1	B1	-------	R126	G126	B126	R127	G127	B127	0	159
3	1	158							-------							1	158
4	2	157							-------							2	157
5	3	156							-------							3	156
6	4	155							-------							4	155
7	5	154							-------							5	154
8	6	153							-------							6	153
9	7	152							-------							7	152
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
154	152	7							-------							152	7
155	153	6							-------							153	6
156	154	5							-------							154	5
157	155	4							-------							155	4
158	156	3							-------							156	3
159	157	2							-------							157	2
160	158	1							-------							158	1
161	159	0							-------							159	0
	CA	MX=' 0 '	0			1			-------	126			127				
		MX=' 1 '	127			126			-------	1			0				

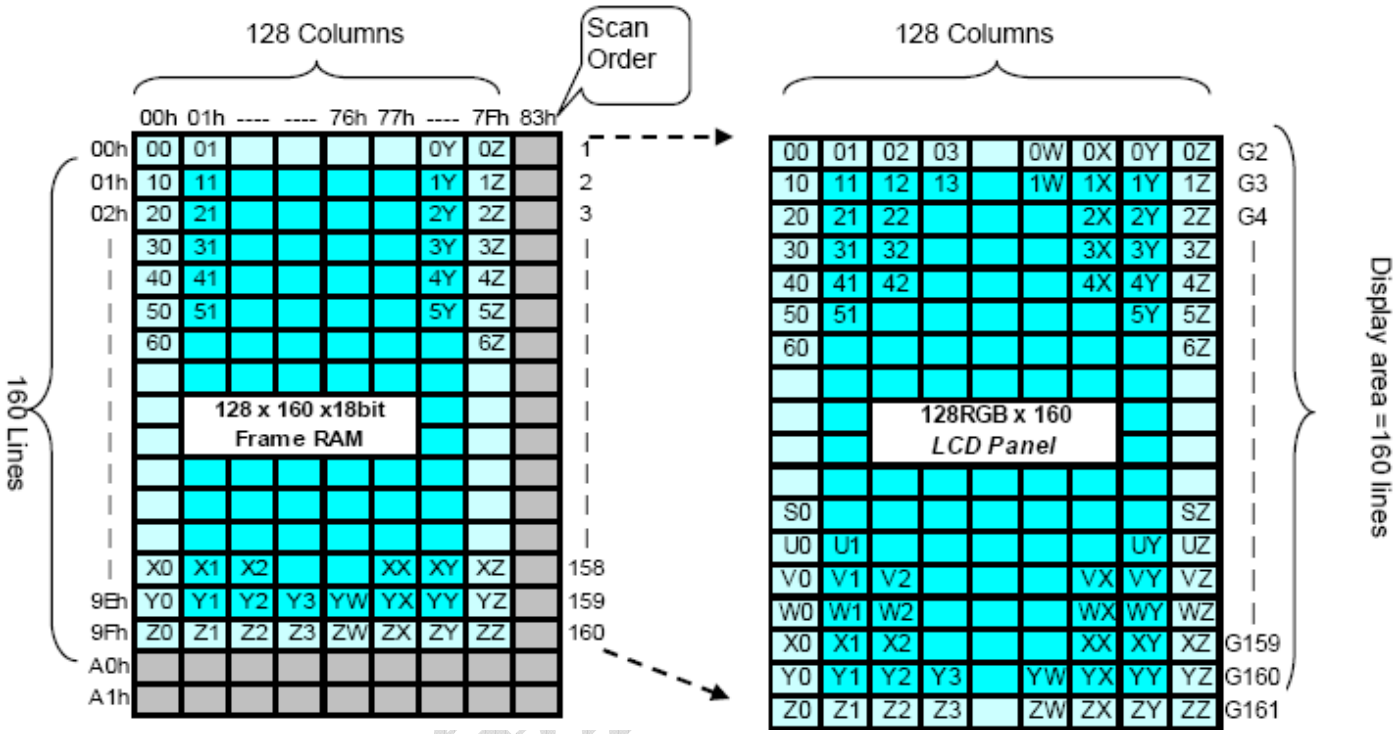
Note
RA = Row Address,
CA = Column Address
SA = Scan Address
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

6.6.3 Normal Display On or Partial Mode On

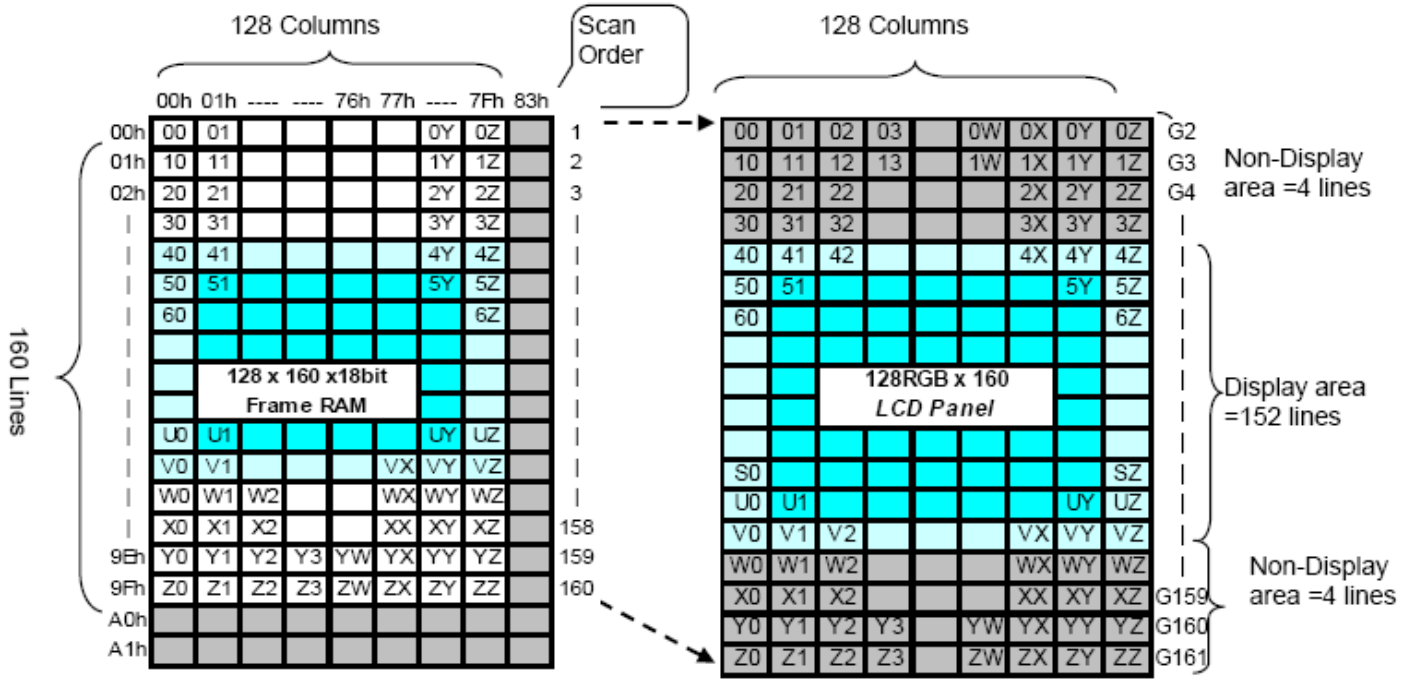
6.6.3.1 When using 128RGB x 160 resolution (GM[2:0] = “011”)

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML=’0’, SMX=SMY=’0’)



2). Example for Partial Display On (PSL[7:0]=04h,PEL[7:0]=9Bh, MX=MV=ML=’0’ ,SMX=SMY=’0’)



6.7 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.
Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit),according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM.The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET and MADCTL” (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.10 below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

6.8 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

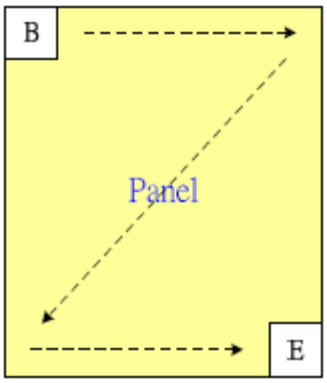


Fig. 6.8.1 Data streaming order

6.8.1 When 128RGBx160 (GM= “011”)

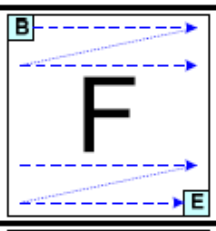
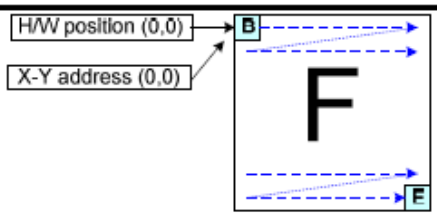
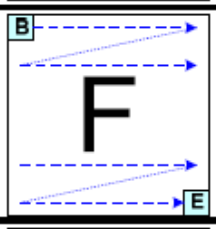
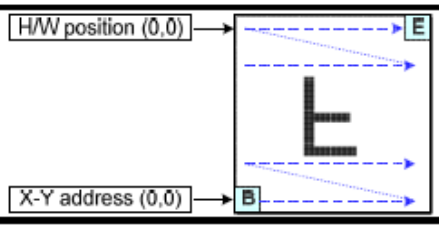
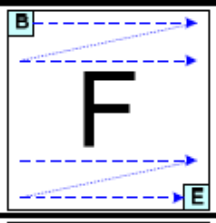
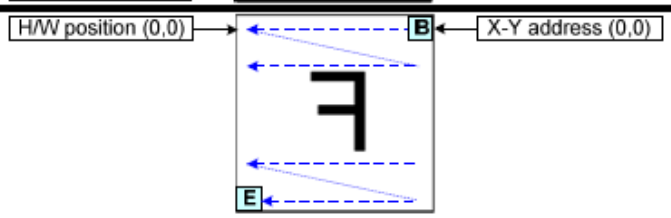
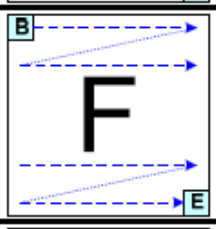
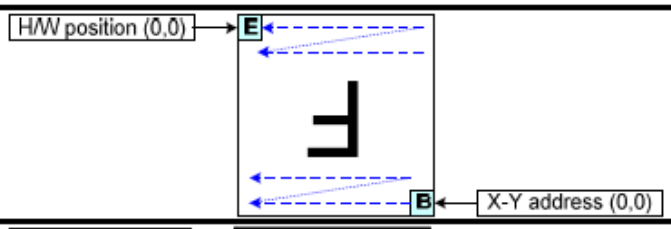
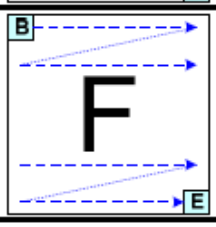
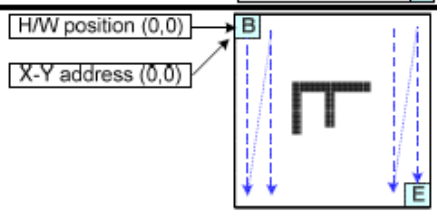
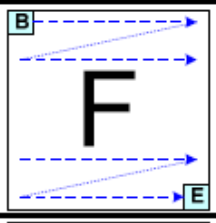
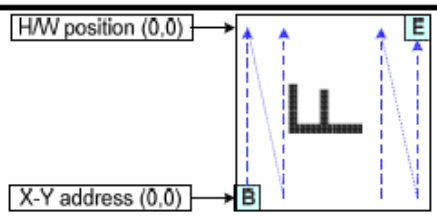
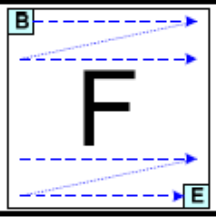
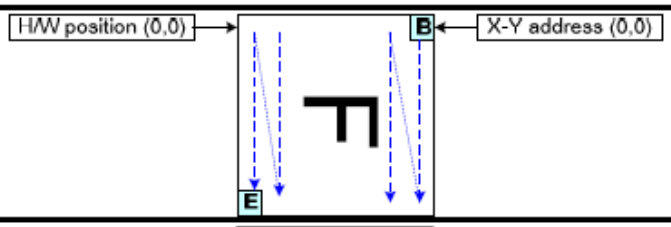
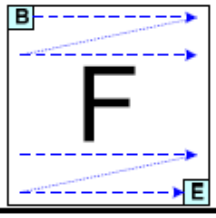
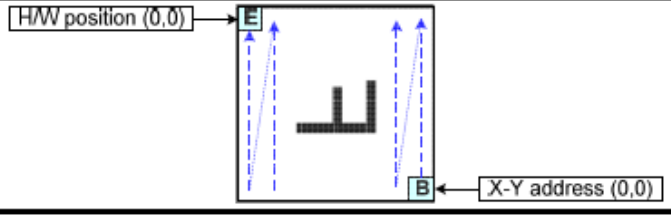
MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7(MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

6.8.2 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

7. Command Table

7.1 System function Command List and Description

Table 7.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	10.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TELOM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	10.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-		-
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-		-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0		-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	TEON	TELOM	-	-	-	-	-	-		-

Table 7.1.2 System Function command List (2)

Instruction	Refer	D/C	WR	RDX	D17-	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	10.1.10	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.12	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	10.1.14	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.16	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.17	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.19	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: 0≦XS≦X
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: S≦XE≦X
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: 0≦YS≦Y
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end:S≦YE≦Y
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	10.1.21	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMRD	10.1.22	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read data

Table 7.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.23	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2, .., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
TEOFF	10.1.24	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.25	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	TELOM		Mode1: TELOM="0" Mode2: TELOM="1"
MADCTL	10.1.26	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		-
IDMOFF	10.1.27	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	10.1.28	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	10.1.29	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface format
RDID1	10.1.30	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	10.1.31	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	10.1.32	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

7.2 Panel Function Command List and Description

Table 7.2.1 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
FRMCTR1	10.2.1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In normal mode (Full colors)
		1	↑	1	-					RTNA3	RTNA2	RTNA1	RTNA0		RTNA set 1-line period FPA: front porch BPA: back porch
		1	↑	1	-			FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
		1	↑	1	-			BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
FRMCTR2	10.2.2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle mode (8-colors)
		1	↑	1	-					RTNB3	RTNB2	RTNB1	RTNB0		RTNB: set 1-line period FPB: front porch BPB: back porch
		1	↑	1	-			FPB5	FPB4	FPB3	FPB2	FPB1	FPB0		
		1	↑	1	-			BPB5	BPB4	BPB3	BPB2	BPB1	BPB0		
FRMCTR3	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In partial mode + Full colors
		1	↑	1	-					RTNC3	RTNC2	RTNC1	RTNC0		RTNC,RTND: set 1-line period FPC,FPD: front porch BPC,BPD: back porch
		1	↑	1	-			FPC5	FPC4	FPC3	FPC2	FPC1	FPC0		
		1	↑	1	-			BPC5	BPC4	BPC3	BPC2	BPC1	BPC0		
		1	↑	1	-					RTND3	RTND2	RTND1	RTND0		
		1	↑	1	-			FPD5	FPD4	FPD3	FPD2	FPD1	FPD0		
		1	↑	1	-			BPD5	BPD4	BPD3	BPD2	BPD1	BPD0		
INVCTR	10.2.4	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display inversion control
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA,NLB,NLC set inversion
DISSET5	10.2.5	0	↑	1	-	1	0	1	1	0	1	1	0	(B6h)	Display function setting
		1	↑	1	-	0	0	NO1	NO0	SDT1	SDT0	EQ1	EQ0		SDT: set amount of source delay EQ: set EQ period PT: No display area source/VCOM/Gate output control
		1	↑	1	-	0	0	0	0	PTG1	PTG0	PT1	PT0		

Table 7.2.2 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PWCTR1	10.2.6	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power control setting
		1	↑	1	-	0	0	0	VRH4	VRH3	VRH2	VRH1	VRH0		VRH: Set the GVDD voltage
		1	↑	1	-	0	1	IB-SEL1	IB-SEL0	0	0	0	0		
PWCTR2	10.2.7	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power control setting
		1	↑	1	-	0	0	0	0	0	BT2	BT1	BT0		BT: set VGH/ VGL voltage
PWCTR3	10.2.8	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In normal mode (Full colors)
		1	↑	1	-	0	0	0	0	0	APA2	APA1	APA0		APA: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCA2	DCA1	DCA0		DCA: adjust the booster Voltage
					-	0	0	0	0	0	0	0	0		
PWCTR4	10.2.9	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle mode (8-colors)
		1	↑	1	-	0	0	0	0	0	APB2	APB1	APB0		APB: adjust the operational amplifier
					-	0	0	0	0	0	0	0	0		
		1	↑	1	-	0	0	0	0	0	DCB2	DCB1	DCB0		DCB: adjust the booster Voltage
					-	0	0	0	0	0	0	0	0		
PWCTR5	10.2.10	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In partial mode + Full colors
		1	↑	1	-	0	0	0	0	0	APC2	APC1	APC0		APC: adjust the operational amplifier
		1	↑	1	-	0	0	0	0	0	DCC2	DCC1	DCC0		DCC: adjust the booster circuit for Idle mode
VMCTR1	10.2.11	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM control 1
		1	↑	1	-	-	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0		VMH: VCOMH voltage control
		1	↑	1	-	-	VML6	VML5	VML4	VML3	VML2	VML1	VML0		VML: VCOML voltage control
VMOFCTR	10.2.12	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	Set VCOM offset control
		1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0		
WRID2	10.2.13	0	↑	1	-	1	1	0	1	0	0	0	1	(D1h)	Set LCM version code
		1	↑	1	-	-	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]		

Table 7.2.3 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRID3	10.2.14	0	↑	1	-	1	1	0	1	0	0	1	0	(D2h)	Customer Project code
		1	↑	1	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Set the project code at ID3
PWCTR6	10.2.15	0	↑	1	-	1	1	1	1	1	1	0	0	(FC)	In partial mode + Idle
		1	↑	1	-	-	Sapa [2]	Sapa [1]	Sapa [0]	---	Sapb [2]	Sapb [1]	Sapb [0]		
		1	↑	1	-	-	Sapc [2]	Sapc [1]	Sapc [0]	---	DCD [2]	DCD [1]	DCD [0]		
NVCTR1	10.2.16	0	↑	1	-	1	1	0	1	1	0	0	1	(D9)	EEPROM control status
		1	↑	1	-	0	0	VMF _EN	ID2 _EN	0	0	0	0		
NVCTR2	10.2.17	0	↑	1	-	1	1	0	1	1	1	1	0	(DEh)	EEPROM Read Command
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	Action code
NVCTR3	10.2.18	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	EEPROM Write Command
		1	↑	1	-	EE_ IB7	EE_ IB6	EE_ IB5	EE_ IB4	EE_ IB3	EE_ IB2	EE_ IB1	EE_ IB0		
		1	↑	1	-	EE_ CMD7	EE_ CMD6	EE_ CMD5	EE_ CMD4	EE_ CMD3	EE_ CMD2	EE_ CMD1	EE_ CMD0		
		1	↑	1	-	1	0	1	0	0	1	0	1	A5	

"-": Don't care

Note 1: The D1h to D3h registers are fixed for about ID code setting.

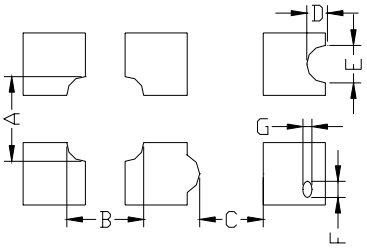
Note 2: The D9h, DEh and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 7.2.4 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
GAMCTRP1	10.2.19	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set
		1	↑	1	-	---	---	VRFP[5]	VRFP[4]	VRFP[3]	VRFP[2]	VRFP[1]	VRF0P[0]		Gamma adjustment (+ polarity)
		1	↑	1	-	---	---	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]		
		1	↑	1	-	---	---	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]		
		1	↑	1	-	---	---	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]		
		1	↑	1	-	---	---	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]		
		1	↑	1	-	---	---	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]		
		1	↑	1	-	---	---	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]		
		1	↑	1	-	---	---	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]		
		1	↑	1	-	---	---	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]		
		1	↑	1	-	---	---	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]		
		1	↑	1	-	---	---	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]		
		1	↑	1		---	---	PKP9[5]	PKP9[4]	PKP9[3]	PKP9[2]	PKP9[1]	PKP9[0]		
		1	↑	1	-	---	---	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]		
		1	↑	1	-	---	---	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]		
		1	↑	1		---	---	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]		
		1	↑	1	-	---	---	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]		
GAMCTRN1	10.2.20	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set
		1	↑	1	-	---	---	VRF0N[5]	VRF0N[4]	VRF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]		Gamma adjustment (- polarity)
		1	↑	1	-	---	---	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]		
		1	↑	1	-	---	---	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]		
		1	↑	1	-	---	---	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]		
		1	↑	1	-	---	---	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]		
		1	↑	1	-	---	---	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]		
		1	↑	1	-	---	---	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]		
		1	↑	1	-	---	---	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]		
		1	↑	1	-	---	---	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]		
		1	↑	1	-	---	---	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]		
		1	↑	1	-	---	---	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]		
		1	↑	1	-	---	---	PKN9[5]	PKN9[4]	PKN9[3]	PKN9[2]	PKN9[1]	PKN9[0]		
		1	↑	1	-	---	---	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]		
		1	↑	1	-	---	---	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]		
		1	↑	1	-	---	---	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]		
		1	↑	1	-	---	---	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]		
EXTCTRL	10.2.21	0	↑	1	-	1	1	1	1	0	0	0	0	(F0h)	Extension Command Control
		1	↑	1	-	0	0	0	0	0	0	0	1	01	
VCOM4L	10.2.22	0	↑	1	-	1	1	1	1	1	1	1	1	(FFh)	Vcom 4 Level control
		1	↑	1	-	TC2[3]	TC2[2]	TC2[1]	TC2[0]	TC1[3]	TC1[2]	TC1[1]	TC1[0]		
		1	↑	1	-	-	-	-	-	TC3[3]	TC3[2]	TC3[1]	TC3[0]		
		1	↑	1	-	0	0	0	1	1	0	1	0		

Note 1: E0-E1 registers are fixed for adjusting Gamma

8. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28 \mid 0<C \mid \frac{D+E}{2}\leq 0.25 \mid \frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor

16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

9. Handling Precautions

9.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

9.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

9.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

9.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

9.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

9.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

9.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.